POD–51EH–C517A–24

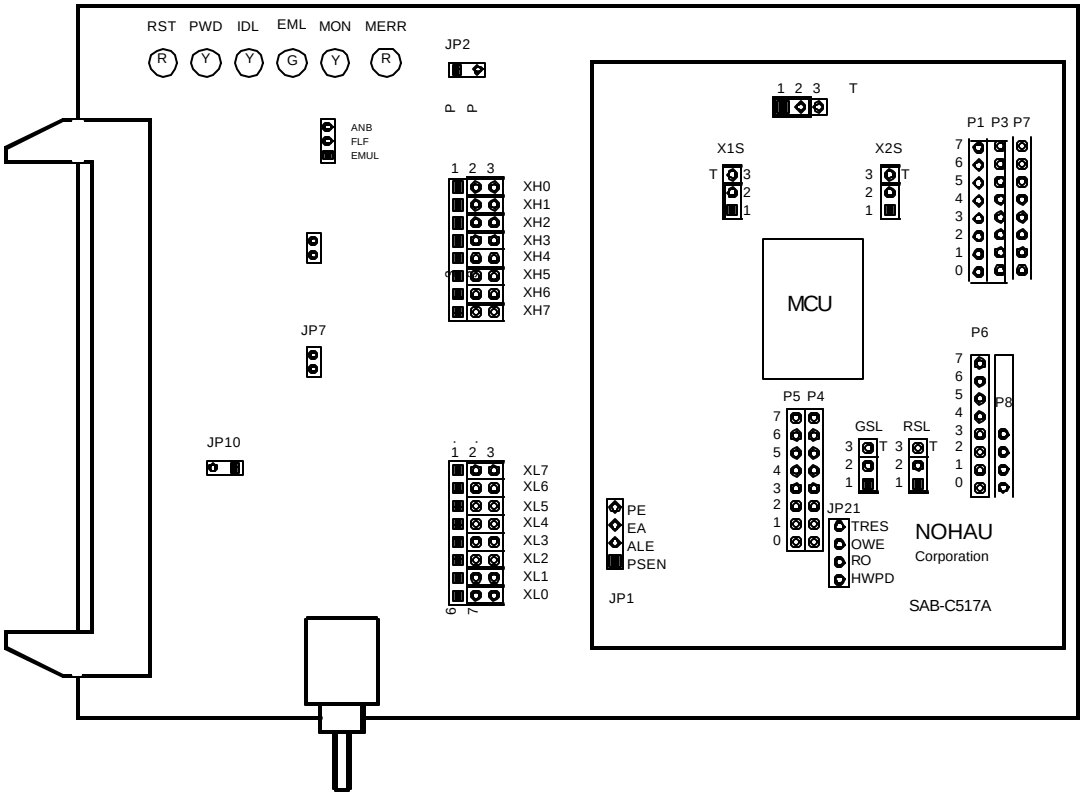

Figure 1. POD–51EH–C517A–24

Operating Instructions

The POD–51EH–C517A–24 supports the Siemens C517A controller which is based on the C500 core.

This pod is supported by the EMUL51–PC Windows software version 2.1M or later. To work with this pod, you need to choose processor C517A in the Hardware Configuration window.

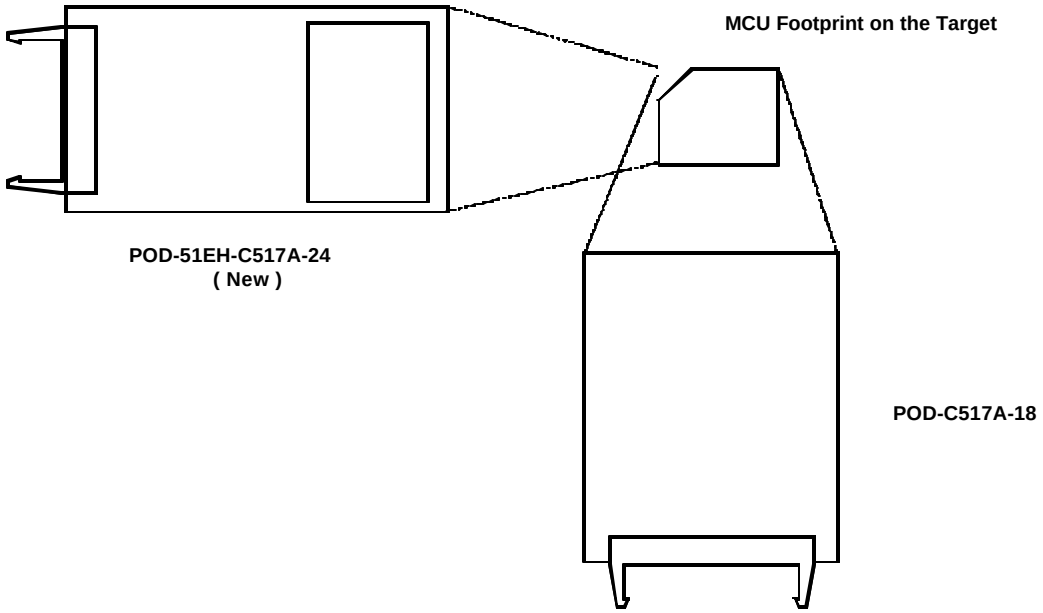

Figure 2. Pod Orientation Relative to the MCU Footprint on the Target

Note: *POD–51EH–C517A–24 replaces POD–C517A–18, an older version of the pod for the Siemens SAB–C517A microcontroller. If you have the older version of the pod, you need to pay attention to the position of the pod relative to your target. Compared to the old pod, the new one needs to turn 90 degrees clockwise when you install it on the same target. (See Figure 2.)*

The EPROM on the emulator board must be version COM 1.4 or later. If it is an older version, you need to replace it with a newer EPROM.

The pod assembly consists of two sub-assemblies. The universal Port Replacement Unit (PRU) is the larger board that carries the small Processor Module (PM) daughterboard.

The PRU has three headers on the bottom that carry the signals to the target. The PRU also has a 50-pin header J1 that connects through the ribbon cable to the emulator board.

The target headers plug into an adapter that you select depending on the type of the controller. For example, the SAB-C517A microcontroller uses the following adapters.

- Emulation Solutions 180–5690–10 (P–MQFP–100)
- Emulation Solutions 180–3975–10 (PLCC–84)

The adapters plug into the target system, replacing the C517A controller IC. These adapters can be ordered from Nohau Corporation or directly from Emulation Solutions.

The POD–51EH–C517A–24 runs up to a maximum frequency of 24 MHz.

The C517A controller has on-chip XRAM memory located at addresses F800H – FFFFH in the data space. If your application uses the on-chip XRAM, you must map the last memory range of the data memory (addresses F000H – FFFFH) to the target.

The EA pin during reset signal rise (also sampled on internal watchdog timer reset) selects the active mode. It is recommended that you connect this pin to either constant low or constant high. This pin defaults to high (selecting single-chip mode), that is implemented by a 22K pull-up resistor on the pin.

POD–51EH–C517A–24 has two operating modes.

- Single-chip
- Expanded

The active mode is selected by the EA pin during reset signal rise (also sampled on internal reset).

When using expanded mode, the code memory can be mapped either to the target or the emulator (with boundaries of 4K). In expanded mode, addresses are seen on the Port2 and Port0 adapter pins for every bus cycle regardless of where it is mapped. The data, however, is read or written to the Port0 pins only for addresses that are mapped to the target.

When using single-chip mode, you need to map all code memory to the emulator board. In this mode, Port2 and Port0 can be used as I/O ports. These adapter pins carry the address and data information only in the following cases.

- XRAM data access to an address that is mapped to the target, or
- XRAM data accesses to the internal XRAM when the XMAP1 bit in the SYSCON register is set.

In all other cases (for example, code access) these pins do not carry the address or data information since all of the code is fetched from the user code memory on the emulator board.

POD–51EH–C517A–24 also supports tracing of internal XRAM read and write cycles using MOVX instructions. This is supported in both single-chip and expanded modes, regardless of the state of the P3.6 and P3.7 recreated signals. These pins are also used for RD and WR signals. The pod enables emulation and tracing of XRAM data writes and reads of the on-chip XRAM and the XRAM on the emulator, while allowing the use of recreated pins P3.6 and P3.7 as I/O pins. This feature does not work correctly for target XRAM, as these two pins are used as RD and WR signals.

It is important to note that:

- The C517A controller has a default watchdog timer running at start-up. We recommend that you disable this watchdog timer by connecting pin PE/WDT to GND. Otherwise, an unexpected reset can occur while debugging is in process.

- The C517A controller cannot wake up from a software power-down made by a low signal at the P3.2/INT0 pin.

Jumpers

Ground SeLect (GSL): VAGND Grounding Select

This jumper selects how to ground the VAGND pin of the controller. When the jumper top is across pins 1 and 2, VAGND is connected to emulator ground. When the jumper top is across pins 2 and 3, VAGND is grounded through pin 4 of the target adapter. The letter T to show connection to the target marks pin 3 of the jumper. The default position of the jumper top is across pins 1 and 2 (emulator ground selected).

Reference SeLect (RSL): VAREF Source Select

This jumper selects how to power the VAREF pin of the controller. When the jumper top is across pins 1 and 2, VAREF is connected to emulator. When the jumper top is across pins 2 and 3, VAREF is connected to the target through pin 3 of the target adapter. The letter T to show connection to the target marks pin 3 of the jumper. The default position of the jumper top is across pins 1 and 2 (emulator selected as the voltage source).

VCC SeLect (VSL): Controller VCC Source Select

This jumper selects how to power the VCC pins of the controller. When the jumper top is on pins 1 and 2, the controller VCC pins are connected to the VCC of the emulator. When the jumper top is on pins 2 and 3, the controller VCC pins are connected to the VCC pins of the adapter. This allows the controller VCC pins to be powered by the target. The default position of the jumper top is across pins 1 and 2 (emulator selected as VCC source).

Note: *Taking power from the target system is* ***not recommended****.*

Note: *Both VCC pins of the controller are shorted together.*

X1S, X2S: XTAL1 and XTAL2 Source Select

These two jumpers select the clock source for the controller. With the jumper tops on pins 1 and 2, the controller XTAL1 and XTAL2 pins are connected to a 24-MHz crystal on the pod. When these two jumpers have jumper tops on pins 2 and 3, the controller XTAL1 and XTAL2 pins are connected to pins 37 and 36 of the adapter. This allows the target to supply the clock to the controller XTAL1 and XTAL2 pins. The default position of the jumper top is across pins 1 and 2 (the pod crystal).

Note: *Both of the jumper tops need to be placed in the same position with either both selecting the pod crystal source, or both selecting the target clock source.*

JP8: Monitor Stop/Break Select

This jumper determines whether all or only part of the internal MCU peripherals stop in monitor mode after an emulation break occurs. When the jumper top is out, the STOP mode is selected. In this case, all of the internal MCU peripherals are stopped in monitor mode. This includes the following controller peripherals.

- Interrupts
- Watchdog timer
- Oscillator watchdog
- Timer0
- Timer1
- Timer2
- Timer2 capture
- CCU compare timer
- USART0
- USART1

When the jumper top is on, the BREAK mode is selected. In this case, only some of the internal peripherals are stopped. This includes the following controller peripherals.

- Interrupts
- Watchdog timer
- Oscillator timer
- Timer2

Timer0, Timer1, Timer2 capture, CCU compare timer, USART0, and USART1 are not stopped in this mode.

In STOP and BREAK, all of the internal peripherals start working from the same point they stopped before the break as soon as the user program starts running again when you press the GO or STEP buttons. When changing this jumper, the new STOP/BREAK mode takes effect

after the next RESET sequence. The default setup of the jumper is STOP mode selection (jumper top out).

Note: *It is recommended to work in STOP mode only. The break mode needs to be selected only if your application has limitations that do not allow the timers to be stopped in monitor mode.*

XL0..XL7: Port Select Jumpers

These eight 3-pin jumpers select the signals that are routed to the trace board and are shown in the trace window under the header P1. For any jumper in this group the jumper top position pin 2–pin 3 means that the corresponding pin of the recreated Port0 is traced. Pin 1 of each jumper is left free and can be connected to any signal on the target or port headers on the pod. For example setting XL4 in position 2–3 means that pin P0.4 is traced. If pin XL4.1, for example, is connected to a signal P4.3 on the target, you can choose between tracing signal P0.4 or P4.3 by moving the jumper between positions 2–3 and 1–2.

XH0..XH7: Port Select Jumpers

This group of jumpers is similar to XL0..XL7, except pin 3 of each jumper is connected to the recreated Port2 and pin 1 is left free.

JP7 (External Code Enable)

This jumper enables access to the external code if the single-chip mode is emulated and part of the code is mapped into the target code memory. The external code is enabled if the jumper top is out (default jumper configuration).

Reset Button

When pressed, this switch resets the pod (including the controller). You can use this button to recover from a map error status. (See the following "Map Error LED" section.)

Reset LED

The Reset LED (red LED) is turned on whenever the microcontroller reset is active. There are five possible sources of the controller reset.

1. Reset from the target starts whenever a low level is detected on the reset pin of the adapter.
2. Reset from the S1 button starts by pressing the S1 button on the pod.
3. Reset from the emulator starts by clicking the reset button in the user interface EMUL51–PC Windows software.
4. Reset from the internal watchdog timer starts if the internal watchdog is enabled, and the user software does not feed it for a long period.

Note: *It is important to feed the watchdog periodically, otherwise, problems during the debug process might occur.*

5. During hardware power-down initiated by a low level detected on pin 69 (HWPD) of the target adapter.

6. When a map error occurs. (See the following "Map Error LED" section.)

During all of these reset sequences, the reset LED is turned on for a short or long period depending on the sequence).

Map Error LED

This red LED signals a mapping error occurring in one of the following situations.

- The internal C517A XRAM is enabled by bit XMAP0 in the SYSCON register, the data memory address range F000H – FFFFH is mapped to the emulator, and there is a memory access (MOVX) to the internal XRAM. This state is illegal. When the C517A internal XRAM is enabled and accesses are made to it, the data memory address range F000H – FFFFH needs to be mapped to the target.

- The EA pin from the target (during the last reset) selects single-chip mode, a code memory address range is mapped to the target, and there is code access to one of the addresses in this range. This state is illegal. In single-chip mode all of the code memory needs to be mapped to the emulator and not to the target, because the 64K code memory is internal to the C517A controller.

If one of these illegal states occurs, the Map Error LED turns on simultaneously with the C517A controller entering the reset state, signaling the illegal state. This state is maintained until you push the reset button. Leaving the map error state is done ***only*** by pressing the reset button S1 on the pod. This prevents repetitive occurrences of the illegal state until you fix the problem.

Emulation LED

The Emulation LED (green LED) turns on whenever the user program is running, and turns off whenever the user program is stopped (emulation break). The user code can be fetched from RAM on the emulator board or from code memory on the target (usually PROM).

Monitor LED

The Monitor LED (yellow LED) turns on whenever the monitor mode is active. In this mode, the controller executes internal emulator code that communicates with the host PC. The emulator enters this mode upon power-up or after emulation break.

Headers

JP10: SY0, SY1

This header contains two pins: Pin 1 (SY0), and pin 2 (SY1). These two signals are carried to the emulator and trace boards, and can be used in the trace and breakpoint logic.

JP9: EMUL, FLF, ANB

This header contains three pins: Pin 1 (EMUL), pin 2 (FLF), and pin 3 (ANB). Pin1 signals emulation or monitor mode. It is low when emulation is active (when the user program is running). Pins 2 and 3 are not used currently, but can be used in the future.

J2: P3.6, P3.7

This header carries the recreated signals: P3.6/WR (pin J2.1) and P3.7/RD (pin J2.2). These pins observe the signals or route them to the trace board through the headers XL0..XL7, XH0..XH7.

JP1: PE, EA, ALE, PSEN

This header carries the signal listed previously and is used for testing, or can be connected to the trace board through the headers XL0..XL7, XH0..XH7.

JP21: RESET, P7.0, CPUR, HWPD

This header carries the signal listed previously and is used for testing, or can be connected to the trace board through the headers XL0..XL7, XH0..XH7.

P1, P3, P4, P5, P6, P7, P8: Port Headers

These headers carry signals for the corresponding ports. The port pin numbers are marked on the silk-screen. For example, pin 5 of header P4 connects to pin P4.5 of the microcontroller.

Differences Between the Emulator and the C517A Microcontroller

The EA Pin—The EA pin is an input pin that during reset, is sampled by the controller in order to select between single-chip mode (program in internal ROM) and expanded mode (program in external memory). This input pin on the controller floats, meaning it does not have a pull-up or pull-down resistor. On the pod a 22K pull-up resistor connects to this pin to select a default state of single-chip mode when the target does not force this pin. This difference must be taken into account if the target pin is tied to a pull-down resistor. A sufficiently low pull-down (1.5K or lower) is required to overcome the 22K pull-up resistor on the pod.

Port0 and Port2 Pins—The pod emulates these 16 port pins, used as the address/data bus and as port pins. These pins have slightly different AC and DC characteristics from the Port0 and Port2 pins of the controller. These pins sink up to 12mA and source up to 4mA, while maintain-

ing valid TTL output logic levels. Port2 pins also have pull-up resistors of 22K, which might be different from the controller internal pull-ups.

Connecting the Pod to a Target System

1. Make sure the power is turned off in both the host PC and the target system.
2. Connect the black EZ-hook from the pod to the target GND.
3. Turn on the power to the PC first, and then turn on the power to the target.
4. When turning the power off, turn off the target power first, and then turn off the PC power.