POD–51EH–C505L–20

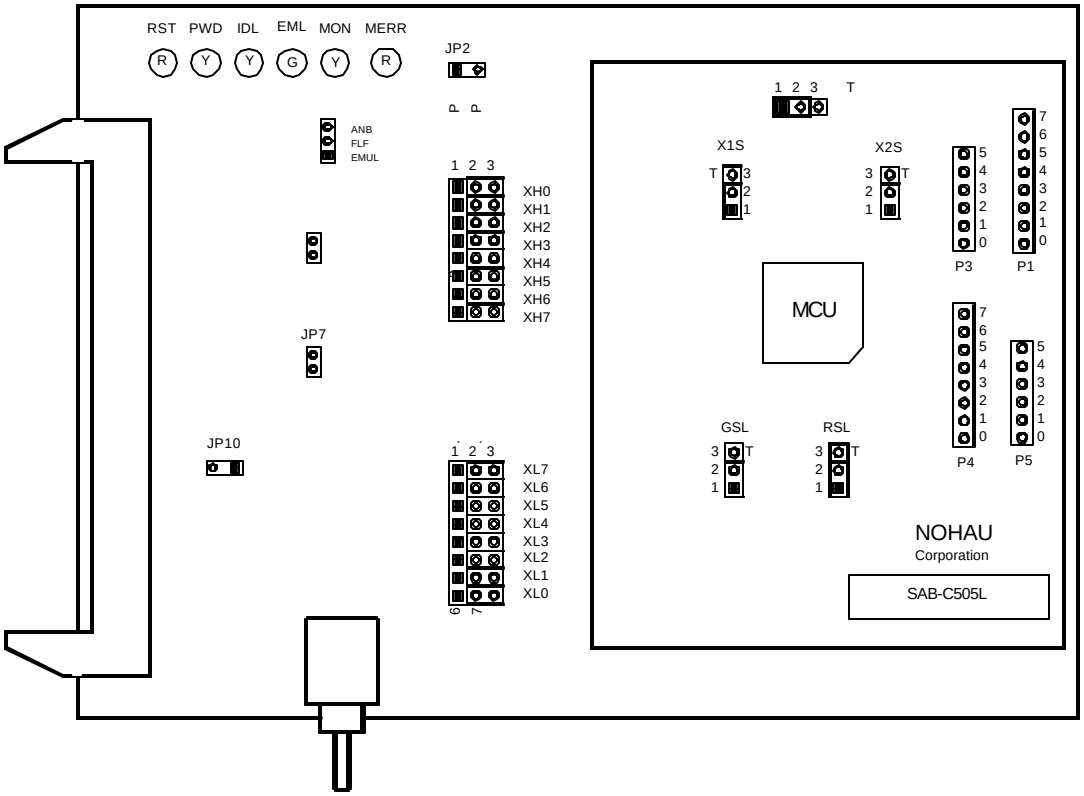

Figure 1. POD–51EH–C505L–20

Operating Instructions

The POD–51EH–C505L–20 supports the Siemens C505L microcontroller.

This pod is supported by the EMUL51–PC Windows software version 2.1J or later. To work with this pod, you need to choose the C505L processor in the Hardware Configuration window.

The EPROM on the emulator board must be version COM 1.4 or later. If it is an older version, you need to replace it with a newer EPROM.

The pod assembly consists of two sub-assemblies. The universal Port Replacement Unit (PRU), is the larger board that carries the small Processor Module (PM) daughterboard.

The target headers plug into an adapter that you select depending on the type of controller. The C505L microcontroller uses the the Emulation Solutions 180–5550–65 adapter.

This is a QFP–80 solder-down adapter that is soldered to the target system, replacing the C505L microcontroller IC. This adapter can be ordered from Nohau Corp. or directly from Emulation Solutions.

The POD–51EH–C505L–20 runs up to a maximum frequency of 20 MHz. It has an internal 16-MHz crystal on the board. In order to work at a frequency higher than 16 MHz, for example, 20 MHz, an external 50% duty cycle clock signal should be supplied from the target board and the jumpers should be configured accordingly. See the "Jumpers" section.

Every operating frequency of the C505L is equivalent to twice the operating frequency of an original 8051 microcontroller with the same clock frequency. For example, when using a 16-MHz crystal the operating frequency is equivalent to an 8051 with a 32-MHz crystal. This is because the C505L doesn't divide the clock source by two as does the original 8051.

For this reason, the POD–51EH–C505L–20 might only function correctly with twice the higher frequency of the emulator and trace boards. For example, for a 16-MHz operation, use an emulator and trace boards with 32 MHz frequency or higher. For a 20-MHz operation, use an emulator and trace boards with 40 MHz frequency or higher.

In addition, you need to input twice the microcontroller frequency in the CLK field in the Hardware Configuration window. For example, for a 20-MHz clock, input 40 MHz in the CLK field.

For details on how to configure the advanced emulator boards for *high frequency operation* with the pod, refer to the "Advanced Emulator Configuration for the Pod" section.

The C505L microcontrollers have 256 bytes of on-chip memory located at XDATA addresses FF00H – FFFFH. The C505L also has the LCD controller registers and real-time clock (RTC) registers mapped to XDATA space at addresses F3DCH – F3FFH. If your application is using the on-chip XRAM or the LCD/RTC registers, you must map the last memory range of the XDATA memory (addresses F000H – FFFFH) to the target. This memory mapping is done under the Config Memory Map menu in the EMUL51–PC Windows software, or the Config Emulator menu in the Seehau software.

POD–51EH–C505L–20 has two operating modes.

- Single-chip
- External

The active mode is selected by the EA pin (pin 29 of the POD–51EH–C505L–20 adapter) during the Reset signal rise (also sampled on internal watchdog timer Reset).

This pin is sampled by the emulator only during Exit from Reset, and therefore, it is recommended that you connect it to either Constant Low or Constant High. This pin defaults to High (selecting single-chip mode), which is implemented by a 47K pull-up resistor on the pin.

When using external mode, the code memory can be mapped either to the target or to the emulator (with boundaries of 4K). In external mode, addresses are switched to Port2 and Port0 pins for every bus cycle regardless of where it is mapped. The data, however, is read or written to the Port0 pins only for addresses that are mapped to the target.

When using single-chip mode, ***you need to map the first 32K of the code memory (address range 0 –7FFFH) to the emulator board***. In this mode, Port2 and Port0 can be used as I/O ports. These pins carry the address and data information only in the following cases.

- XDATA accesses, using MOVX instructions, to an address that is mapped to the target.
- XDATA accesses to the internal XRAM when the XMAP1 bit in the SYSCON register is set.
- Depending on JP7, for code accesses—see details in the "JP7: External Code Enable" section.

In all other cases, depending on JP7, these pins carry I/O values of Port0 and Port2 either out-putted from the microcontroller according to the Port0 and Port2 SFR registers value, or in-putted from the target to the microcontroller.

Jumpers

Ground SeLect (GSL): VAGND Grounding Select

This jumper selects how to ground the VAGND pin of the controller. When the jumper top is across pins 1 and 2, VAGND is connected to emulator ground. When the jumper top is across pins 2 and 3, VAGND is grounded to the target. Pin 3 of the jumper is marked by the letter T to show connection to the target. The default position of the jumper top is across pins 1 and 2 (emulator ground selected).

Reference SeLect (RSL): VAREF Source Select

This jumper selects how to power the VAREF pin of the controller. When the jumper top is across pins 1 and 2, VAREF is connected to emulator. When the jumper top is across pins 2 and 3, VAREF is connected to the target. Pin 3 of the jumper is marked by the letter T to show connection to the target. The default position of the jumper top is across pins 1 and 2 (emulator selected as the voltage source).

VCC SeLect (VSL): Controller VCC Source Select

This jumper selects how to power the VCC pin of the controller. When the jumper top is on pins 1 and 2, the controller VCC pin is connected to the VCC of the emulator. When the jumper top is on pins 2 and 3, the controller VCC pin is connected to the VCC pin of the adapter. This allows the controller VCC pin to be powered by the target. The default position of the jumper top is across pins 1 and 2 (emulator selected as VCC source).

Note: *Taking power from the target system is* ***not recommended****.*

X1S, X2S: XTAL1 and XTAL2 Source Select

These two jumpers select the clock source for the controller. With the jumper tops on pins 1 and 2, the controller XTAL1 and XTAL2 pins are connected to a 16-MHz crystal on the pod. When these two jumpers have jumper tops on pins 2 and 3, the controller XTAL1 and XTAL2 pins are connected to the target. This allows the target to supply the clock to the controller XTAL1 and XTAL2 pins. The default position of the jumper top is across pins 1 and 2 (the pod crystal).

Note: *Both of the jumper tops need to be placed in the same position with either both selecting the pod crystal source, or both selecting the target clock source.*

JP8: Monitor Stop / Break Select

This jumper determines whether all or only part of the internal MCU peripherals stop in monitor mode after an emulation break occurs. When the jumper top is out, the STOP mode is selected. In this case, all of the internal MCU peripherals are stopped in monitor mode. This includes the following microcontroller peripherals.

- Interrupts
- Oscillator Watchdog
- Timer0
- Timer1
- Timer2
- USART

When the jumper top is on, the BREAK mode is selected. In this case, only some of the internal peripherals are stopped. This includes the following microcontroller peripherals.

- Interrupts
- Oscillator Watchdog
- Timer2

Timer0, Timer1, and USART are not stopped in this mode.

In STOP and BREAK, all of the internal peripherals start working from the same point they stopped before the break as soon as the user program starts running again when you press GO or STEP.

When changing this jumper, the new STOP/BREAK mode takes effect after the next RESET sequence. The default setup of the jumper is STOP mode selection (jumper top out).

Note: *It is recommended to work in STOP mode only. The break mode needs to be selected only if your application has limitations that do not allow the timers to be stopped in monitor mode.*

XL0..XL7: Port Select Jumpers

These eight 3-pin jumpers select the signals that are routed to the trace board and are shown in the trace window under the header P1. For any jumper in this group the jumper top position pin 2–pin 3 means that the corresponding pin of the recreated Port0 is traced. pin 1 of each jumper is left free and can be connected to any signal on the target or port headers on the pod. For example setting XL4 in position 2–3 means that pin P0.4 is traced. If pin XL4.1, for example, is connected to a signal P4.3 on the target, you can choose between tracing signal P0.4 or P4.3 by moving the jumper between positions 2–3 and 1–2.

XH0..XH7: Port Select Jumpers

This group of jumpers is similar to XL0..XL7, except pin 3 of each jumper is connected to the recreated Port2 and pin 1 is left free.

JP7: External Code Enable

This jumper enables access to the external code if the single-chip mode is emulated and part of the code is mapped into the target code memory. The external code is enabled if the jumper top is out (default jumper configuration).

Reset Button

When pressed, this switch resets the pod (including the controller). You can use this button to recover from a map error status. (See the "Map Error LED" section.)

Reset LED

The Reset LED (red LED) is turned on whenever the microcontroller reset is active. There are five possible sources of the controller reset.

1. Reset from the target starts whenever a low level is detected on the reset pin of the adapter.
2. Reset from the S1 button starts by pressing S1 on the pod.
3. Reset from the emulator starts by clicking the reset button in the user interface EMUL51–PC Windows software.
4. When a map error occurs. (See the "Map Error LED" section.)

During all of these reset sequences, the reset LED is turned on for a short or a long period of time depending on the sequence.

Map Error LED

This red LED signals a mapping error occurring in one of the following situations.

When the internal C505L XRAM is enabled by bit XMAP0 in the SYSCON register, the data memory address range FF00H – FFFFH is mapped to the emulator, and there is a memory access (MOVX) to the internal XRAM. This state is illegal. When the C505L internal XRAM is enabled and accesses are made to it, the data memory address range FF00H – FFFFH ***needs to be mapped to the target***.

When single-chip mode is selected by the EA pin from the target during the last Reset, a code memory address range in the first 32K (address 0 – 7FFFH) is mapped to the target and there is code access to one of the addresses in this range. This state is illegal. In single-chip mode, when JP7 is set to disable code accesses to the target, all code memory needs to be mapped to the emulator.

If one of these illegal states occurs, the Map Error (ERR) LED turns on simultaneously with the C505L microcontroller on the pod entering the reset state, signaling the illegal state. This state is maintained until you push the reset button. Leaving the map error state is done ***only*** by pressing the reset button S1 on the pod. This prevents repetitive occurrences of the illegal state until you fix the problem.

Emulation LED

The Emulation LED (green LED) turns on whenever the user program is running, and turns off whenever the user program is stopped (emulation break). The user code can be fetched from RAM on the emulator board or from code memory on the target (usually PROM).

Monitor LED

The Monitor LED (yellow LED) turns on whenever the monitor mode is active. In this mode, the controller executes internal emulator code that communicates with the host PC. The emulator enters this mode upon power-up or after emulation break.

Headers

JP10—SY0, SY1

This header contains two pins; pin 1 (SY0), and pin 2 (SY1). These two signals are carried to the emulator and trace boards, and can be used in the trace and breakpoint logic.

JP9—EMUL, FLF, ANB

This header contains three pins: pin 1 (EMUL), pin 2 (FLF), and pin 3 (ANB). Pin 1 signals emulation or monitor mode. It is low when emulation is active (when the user program is running). Pins 2 and 3 are not used currently, but can be used in the future.

J2: P3.6, P3.7

This header carries the recreated signals; P3.6/WR (Pin J2.1) and P3.7/RD (pin J2.2). These pins observe the signals or route them to the trace board through the headers XL0..XL7, XH0..XH7.

P1, P3, P4, P5: Port Headers

These headers carry signals for the corresponding ports. The port pin numbers are marked on the silk-screen. For example, pin 5 of header P3 connects to pin P3.5 of the microcontroller.

Advanced Emulator Configuration for the Pod

When using an advanced emulator board (part numbers EMUL51–PC/EA256–BSW–50 or the EMUL51–PC/EA768–BSW–50), it is important to configure the advanced emulator board for the POD–C505L, especially when applying a high frequency clock signal above 12 MHz to the C505L microcontroller.

Make sure that the two following jumpers in the advanced emulator board ***are removed***.

- The DAL jumper on JP1
- The RWEN jumper on JP1

These two jumpers affect the operation mode and maximum operating frequency of the advanced emulator board.

For details on how to configure the other jumpers on the advanced emulator board, refer to the *EMUL51–PC User's Guide*.

The Differences between the Emulator and the C505L Microcontroller

This section describes the difference between the behavior of the C505L emulator and the C505L microcontroller chip.

EA Pin

The EA pin in the C505L microcontroller is an input pin used to select between single-chip mode (the program in internal OTP–ROM) and external mode (the program in external memory). This pin on the C505L microntroller is an input and is floating. It does not have a pull-up or a pull-down resistor.

On the pod, a 47K pull-up resistor is connected to this pin to select a default state of single-chip mode when this pin is not forced by the target.

This difference of the existence of the pull-up resistor must be taken into account, since if the target pin is to be tied to a pull-down resistor, it should be a sufficiently low pull-down (3.3K or lower) in order to overcome the 47K pull-up resistor on the pod.

Port0 and Port2 Pins

These 16 port pins, used as the address/data bus and as port pins, are emulated by the pod. These pins have slightly different AC and DC characteristics from the Port0 and Port2 pins of the C505L microcontroller. These pins sink up to 12mA and source up to 4mA, while maintaining valid TTL output logic levels. Port2 pins also have pull-up resistors of 22K, which might be different from the C505L microcontroller's internal pull-ups.

Port3.3/WR and Port3.7/RD Pins

These 16 port pins, used as the read and write signals or port pins, are emulated by the pod. These pins have slightly different AC and DC characteristics from the Port3.6/WR and Port3.7/RD pins of the C505L microcontroller. These pins sink up to 12mA and source up to 4mA, (on transition from logic 0 to 1) while maintaining valid TTL output logic levels. These pins also have pull-up resistors of 22K, (to maintain a logic 1 level and emulate the quasi-bi-directional operation) which might be different from the internal pull-ups of the C505L microcontroller.

Connecting the Pod to a Target System

1. Make sure the power is turned off in both the host PC and the target system.
2. Connect the black EZ-hook from the pod to the target GND.
3. Turn on the power to the PC first, and then turn on the power to the target.
4. When turning the power off, turn off the target power first, and then turn off the PC power.