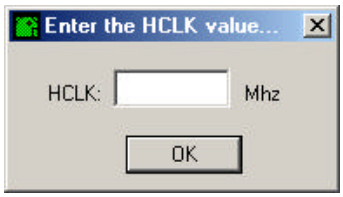
Application Note

Initializing the SDRAM Controller
on the Nohau LPC3000 Evaluation Board

The below macro will demonstrate how to initialize the SDRAM controller on the Nohau LPC3000 Evaluation board.

This macro is downloadable from http://www.nohau.com/sftw/arm/sdram_initialization_hclk_xxxmhz.zip

When the macro is run you will see the following dialog box pop-up asking for an entry if the frequency of the HCLK in Mhz.



By entering the frequency the macro will adjust for the communication operation to initialize the SDRAM controller allowing you to read and modify values in the SDRAM memory through the Seehau interface's DATA window(s).

Example Macro:

```
Sub Main
 '
 ' Philips LPC3000 Evaluation Board SDRAM ( Two Micron MT48H8M16LFB4-8 ) Initialization Macro
 ' HCLK = xxxMHz
 '

 Dim rslt As Long
 Dim hclk As Double

        Begin Dialog UserDialog 250,77,"Enter the HCLK value..." ' %GRID:10,7,1,1
                Text 30,21,50,14,"HCLK:",.Text1
                TextBox 80,14,90,21,.HclkMhz
                Text 180,21,40,14,"Mhz",.Text2
                OKButton 90,49,90,21
        End Dialog
        Dim dlg As UserDialog
        Dialog dlg
        hclk = Val(dlg.HclkMhz)


 'Initialize SDRAM Clock Control Register (SDRAMCLK_CTRL - 0x4000 4068)
 'Bit 0 = 2_0 ; SDRAM HCLK and Inverted HCLK enabled
 'Bit 1 = 2_0 ; DDR_SEL -> SDR SDRAM is used
 'Bit 6:2 = 2_00000 ; DDR_DQSIN_DELAY = 2_00000 * 0.25ns
 'Bit 7 = 2_0 ; RTC_TICK_EN -> No automatic DDR delay calibration
 'Bit 8 = 2_0 ; SW_DDR_CAL -> No manual DDR delay calibration
 'Bit 9 = 2_0 ; CAL_DELAY -> Use uncalibrated delay settings for DDR SDRAM
 'Bit 12:10 = 2_000 ; Sensitivity Factor for DDR SDRAM calibration -> No right shift
 'Bit 13 = 2_0 ; Delay circuitry Adder status -> No overflow or sign bit
 'Bit 18:14 = 2_00111 ; HCLKDELAY_DELAY = 2_00111 * 0.25ns
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'Bit 19 = 2_0 ; SW_DDR_RESET -> No SDRAM ctrl reset
'Bit 20 = 2_0 ; SDRAM_PIN_SPEED1 -> Fast slew rate
'Bit 21 = 2_0 ; SDRAM_PIN_SPEED2 -> Fast slew rate
'Bit 22 = 2_0 ; SDRAM_PIN_SPEED3 -> Fast slew rate
Data_DestSpace "CODE & DATA"
Data_DestAddr "40004068"
Data_SetDWord "0001C000"

'Initialize SDRAM Controller Control Register (MPMCControl - 0x3108 0000)
'Normal Mode, Enabled
'Bit 0 = 2_ 1 ; SDRAM Controller Enable(E) -> Enabled
'Bit 2 = 2_ 0 ; Low-power mode(L) -> Normal
Data_DestSpace "CODE & DATA"
Data_DestAddr "31080000"
Data_SetDWord "00000001"

'Initialize SDRAM Controller Configuration Register (MPMCConfig - 0x3108 0008)
'Bit 0 = 2_ 0 ; 0 Endian mode(N) -> Little-endian mode
Data_DestSpace "CODE & DATA"
Data_DestAddr "31080008"
Data_SetDWord "00000000"

'Initialize SDRAM Controller AHB Control Registers (MPMCAHBControl0 - 0x3108 0400)
'Bit 0 = 2_ 1 ; AHB Port Buffer Enable(E) -> Enable buffer
Data_DestSpace "CODE & DATA"
Data_DestAddr "31080400"
Data_SetDWord "00000001"

'Initialize SDRAM Controller AHB Control Registers (MPMCAHBControl2 - 0x3108 0440)
'Bit 0 = 2_ 1 ; AHB Port Buffer Enable(E) -> Enable buffer
Data_DestSpace "CODE & DATA"
Data_DestAddr "31080440"
Data_SetDWord "00000001"

'Initialize SDRAM Controller AHB Control Registers (MPMCAHBControl3 - 0x3108 0460)
'Bit 0 = 2_ 1 ; AHB Port Buffer Enable(E) -> Enable buffer
Data_DestSpace "CODE & DATA"
Data_DestAddr "31080460"
Data_SetDWord "00000001"

'Initialize SDRAM Controller AHB Control Registers (MPMCAHBControl4 - 0x3108 0480)
'Bit 0 = 2_ 1 ; AHB Port Buffer Enable(E) -> Enable buffer
Data_DestSpace "CODE & DATA"
Data_DestAddr "31080480"
Data_SetDWord "00000001"

'Initialize Dynamic Memory Configuration Register (MPMCDynamicConfig0 - 0x3108 0100)
'Bit 2:0 = 2_010 ; Memory device(MD) -> Low power SDR SDRAM
'Bit 14:7 = 2_ 10101001 ; Address mapping(AM) -> 32-bit external bus low-power SDRAM address
mapping :
'                                    128Mb (8Mx16), 4 banks, row length = 12, column length = 9
'Bit 20 = 2_0 ; Write protect(P) -> Writes not protected
Data_DestSpace "CODE & DATA"
Data_DestAddr "31080100"
Data_SetDWord "00005482"
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If ( hclk <= 13) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0001 ; RAS latency(Active to Read/Write delay)(RAS) -> 1 clock cycles
  '                This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000301"
ElseIf ( hclk > 13) And ( hclk <= 26) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0001 ; RAS latency(Active to Read/Write delay)(RAS) -> 1 clock cycles
  '                This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000301"
ElseIf ( hclk > 26) And ( hclk <= 39) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0001 ; RAS latency(Active to Read/Write delay)(RAS) -> 1 clock cycles
  '                This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000301"
ElseIf ( hclk > 39) And ( hclk <= 52) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0010 ; RAS latency(Active to Read/Write delay)(RAS) -> 2 clock cycles
  '                This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000302"
ElseIf ( hclk > 52) And ( hclk <= 65) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0010 ; RAS latency(Active to Read/Write delay)(RAS) -> 2 clock cycles
  '                This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000302"
ElseIf ( hclk > 65) And ( hclk <= 78) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0010 ; RAS latency(Active to Read/Write delay)(RAS) -> 2 clock cycles
  '                This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000302"
ElseIf ( hclk > 78) And ( hclk <= 91) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0010 ; RAS latency(Active to Read/Write delay)(RAS) -> 2 clock cycles
  '                This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000302"
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  Else
    'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
    'Bit 3:0 = 2_0011 ; RAS latency(Active to Read/Write delay)(RAS) -> 3 clock cycles
    '               This value is normally found in SDRAM data sheets as tRCD
    'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080104"
    Data_SetDWord "00000303"
  End If

  'Initialize Dynamic Memory Read Configuration Register (MPMCDynamicReadConfig - 0x3108 0028)
  'Bit 1:0 = 2_01 ; SDR-SDRAM read data strategy(SRD) -> Command delayed strategy, using
MPMCCLKDELAY (command delayed, clock out not delayed)
  'Bit 4 = 2_ 1 ; SDR-SDRAM read data capture polarity(SRP) -> data captured on the positive edge of
HCLK
  'Bit 9:8 = 2_00 ; DDR SDRAM read data strategy(DRD) -> clock out delayed strategy, using RAM_CLK
(command not delayed, clock out delayed)
  'Bit 12 = 2_0 ; DDR SDRAM read data capture polarity(DRP) ->
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080028"
  Data_SetDWord "00000011"

  If ( hclk <= 13) Then
    'Initialize Dynamic Memory Precharge Command Period Register (MPMCDynamictRP - 0x3108 0030)
    'Bit 3:0 = 2_0000 ; Precharge command period(tRP) -> 1 clock cycles
    '               This value is normally found in SDRAM data sheets as tRP
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080030"
    Data_SetDWord "00000000"
  ElseIf ( hclk > 13) And ( hclk <= 26) Then
    'Initialize Dynamic Memory Precharge Command Period Register (MPMCDynamictRP - 0x3108 0030)
    'Bit 3:0 = 2_0000 ; Precharge command period(tRP) -> 1 clock cycles
    '               This value is normally found in SDRAM data sheets as tRP
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080030"
    Data_SetDWord "00000000"
  ElseIf ( hclk > 26) And ( hclk <= 39) Then
    'Initialize Dynamic Memory Precharge Command Period Register (MPMCDynamictRP - 0x3108 0030)
    'Bit 3:0 = 2_0000 ; Precharge command period(tRP) -> 1 clock cycles
    '               This value is normally found in SDRAM data sheets as tRP
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080030"
    Data_SetDWord "00000000"
  ElseIf ( hclk > 39) And ( hclk <= 52) Then
    'Initialize Dynamic Memory Precharge Command Period Register (MPMCDynamictRP - 0x3108 0030)
    'Bit 3:0 = 2_0001 ; Precharge command period(tRP) -> 2 clock cycles
    '               This value is normally found in SDRAM data sheets as tRP
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080030"
    Data_SetDWord "00000001"
  ElseIf ( hclk > 52) And ( hclk <= 65) Then
    'Initialize Dynamic Memory Precharge Command Period Register (MPMCDynamictRP - 0x3108 0030)
    'Bit 3:0 = 2_0001 ; Precharge command period(tRP) -> 2 clock cycles
    '               This value is normally found in SDRAM data sheets as tRP
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080030"
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  Data_SetDWord "00000001"
 ElseIf ( hclk > 65) And ( hclk <= 78) Then
  'Initialize Dynamic Memory Precharge Command Period Register (MPMCDynamictRP - 0x3108 0030)
  'Bit 3:0 = 2_0001 ; Precharge command period(tRP) -> 2 clock cycles
  '               This value is normally found in SDRAM data sheets as tRP
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080030"
  Data_SetDWord "00000001"
 ElseIf ( hclk > 78) And ( hclk <= 91) Then
  'Initialize Dynamic Memory Precharge Command Period Register (MPMCDynamictRP - 0x3108 0030)
  'Bit 3:0 = 2_0001 ; Precharge command period(tRP) -> 2 clock cycles
  '               This value is normally found in SDRAM data sheets as tRP
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080030"
  Data_SetDWord "00000001"
 Else
  'Initialize Dynamic Memory Precharge Command Period Register (MPMCDynamictRP - 0x3108 0030)
  'Bit 3:0 = 2_0010 ; Precharge command period(tRP) -> 3 clock cycles
  '               This value is normally found in SDRAM data sheets as tRP
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080030"
  Data_SetDWord "00000002"
 End If

 If ( hclk <= 13) Then
  'Initialize Dynamic Memory Active to Precharge Command Period Register (MPMCDynamictRAS -
0x3108 0034)
  'Bit 3:0 = 2_0000 ; Active to precharge Command period (tRAS) -> 1 clock cycles
  '               This value is normally found in SDRAM data sheets as tRAS
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080034"
  Data_SetDWord "00000000"
 ElseIf ( hclk > 13) And ( hclk <= 26) Then
  'Initialize Dynamic Memory Active to Precharge Command Period Register (MPMCDynamictRAS -
0x3108 0034)
  'Bit 3:0 = 2_0001 ; Active to precharge Command period (tRAS) -> 2 clock cycles
  '               This value is normally found in SDRAM data sheets as tRAS
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080034"
  Data_SetDWord "00000001"
 ElseIf ( hclk > 26) And ( hclk <= 39) Then
  'Initialize Dynamic Memory Active to Precharge Command Period Register (MPMCDynamictRAS -
0x3108 0034)
  'Bit 3:0 = 2_0010 ; Active to precharge Command period (tRAS) -> 3 clock cycles
  '               This value is normally found in SDRAM data sheets as tRAS
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080034"
  Data_SetDWord "00000002"
 ElseIf ( hclk > 39) And ( hclk <= 52) Then
  'Initialize Dynamic Memory Active to Precharge Command Period Register (MPMCDynamictRAS -
0x3108 0034)
  'Bit 3:0 = 2_0010 ; Active to precharge Command period (tRAS) -> 3 clock cycles
  '               This value is normally found in SDRAM data sheets as tRAS
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080034"
  Data_SetDWord "00000002"
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  ElseIf ( hclk > 52) And ( hclk <= 65) Then
    'Initialize Dynamic Memory Active to Precharge Command Period Register (MPMCDynamictRAS -
0x3108 0034)
    'Bit 3:0 = 2_0011 ; Active to precharge Command period (tRAS) -> 4 clock cycles
    '              This value is normally found in SDRAM data sheets as tRAS
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080034"
    Data_SetDWord "00000003"
  ElseIf ( hclk > 65) And ( hclk <= 78) Then
    'Initialize Dynamic Memory Active to Precharge Command Period Register (MPMCDynamictRAS -
0x3108 0034)
    'Bit 3:0 = 2_0100 ; Active to precharge Command period (tRAS) -> 5 clock cycles
    '              This value is normally found in SDRAM data sheets as tRAS
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080034"
    Data_SetDWord "00000004"
  ElseIf ( hclk > 78) And ( hclk <= 91) Then
    'Initialize Dynamic Memory Active to Precharge Command Period Register (MPMCDynamictRAS -
0x3108 0034)
    'Bit 3:0 = 2_0100 ; Active to precharge Command period (tRAS) -> 5 clock cycles
    '              This value is normally found in SDRAM data sheets as tRAS
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080034"
    Data_SetDWord "00000004"
  Else
    'Initialize Dynamic Memory Active to Precharge Command Period Register (MPMCDynamictRAS -
0x3108 0034)
    'Bit 3:0 = 2_0101 ; Active to precharge Command period (tRAS) -> 6 clock cycles
    '              This value is normally found in SDRAM data sheets as tRAS
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080034"
    Data_SetDWord "00000005"
  End If

  If ( hclk <= 13) Then
    'Initialize Dynamic Memory Self-refresh Exit Time Register (MPMCDynamictSREX - 0x3108 0038)
    'Bit 6:0 = 2_0000001 ; Self-refresh exit Time(tSREX) -> 2 clock cycles
    '                This value is normally found in SDRAM data sheets as tSREX
    '                For devices without this parameter you use the same value as tXSR
    '                For some DDR-SDRAM data sheets, this parameter is known as tXSNR
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080038"
    Data_SetDWord "00000001"
  ElseIf ( hclk > 13) And ( hclk <= 26) Then
    'Initialize Dynamic Memory Self-refresh Exit Time Register (MPMCDynamictSREX - 0x3108 0038)
    'Bit 6:0 = 2_0000010 ; Self-refresh exit Time(tSREX) -> 3 clock cycles
    '                This value is normally found in SDRAM data sheets as tSREX
    '                For devices without this parameter you use the same value as tXSR
    '                For some DDR-SDRAM data sheets, this parameter is known as tXSNR
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080038"
    Data_SetDWord "00000002"
  ElseIf ( hclk > 26) And ( hclk <= 39) Then
    'Initialize Dynamic Memory Self-refresh Exit Time Register (MPMCDynamictSREX - 0x3108 0038)
    'Bit 6:0 = 2_0000011 ; Self-refresh exit Time(tSREX) -> 4 clock cycles
    '                This value is normally found in SDRAM data sheets as tSREX
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  '                 For devices without this parameter you use the same value as tXSR
  '                 For some DDR-SDRAM data sheets, this parameter is known as tXSNR
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080038"
  Data_SetDWord "00000003"
ElseIf ( hclk > 39) And ( hclk <= 52) Then
  'Initialize Dynamic Memory Self-refresh Exit Time Register (MPMCDynamictSREX - 0x3108 0038)
  'Bit 6:0 = 2_0000100 ; Self-refresh exit Time(tSREX) -> 5 clock cycles
  '                 This value is normally found in SDRAM data sheets as tSREX
  '                 For devices without this parameter you use the same value as tXSR
  '                 For some DDR-SDRAM data sheets, this parameter is known as tXSNR
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080038"
  Data_SetDWord "00000004"
ElseIf ( hclk > 52) And ( hclk <= 65) Then
  'Initialize Dynamic Memory Self-refresh Exit Time Register (MPMCDynamictSREX - 0x3108 0038)
  'Bit 6:0 = 2_0000101 ; Self-refresh exit Time(tSREX) -> 6 clock cycles
  '                 This value is normally found in SDRAM data sheets as tSREX
  '                 For devices without this parameter you use the same value as tXSR
  '                 For some DDR-SDRAM data sheets, this parameter is known as tXSNR
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080038"
  Data_SetDWord "00000005"
ElseIf ( hclk > 65) And ( hclk <= 78) Then
  'Initialize Dynamic Memory Self-refresh Exit Time Register (MPMCDynamictSREX - 0x3108 0038)
  'Bit 6:0 = 2_0000110 ; Self-refresh exit Time(tSREX) -> 7 clock cycles
  '                 This value is normally found in SDRAM data sheets as tSREX
  '                 For devices without this parameter you use the same value as tXSR
  '                 For some DDR-SDRAM data sheets, this parameter is known as tXSNR
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080038"
  Data_SetDWord "00000006"
ElseIf ( hclk > 78) And ( hclk <= 91) Then
  'Initialize Dynamic Memory Self-refresh Exit Time Register (MPMCDynamictSREX - 0x3108 0038)
  'Bit 6:0 = 2_0000111 ; Self-refresh exit Time(tSREX) -> 8 clock cycles
  '                 This value is normally found in SDRAM data sheets as tSREX
  '                 For devices without this parameter you use the same value as tXSR
  '                 For some DDR-SDRAM data sheets, this parameter is known as tXSNR
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080038"
  Data_SetDWord "00000007"
Else
  'Initialize Dynamic Memory Self-refresh Exit Time Register (MPMCDynamictSREX - 0x3108 0038)
  'Bit 6:0 = 2_0001000 ; Self-refresh exit Time(tSREX) -> 9 clock cycles
  '                 This value is normally found in SDRAM data sheets as tSREX
  '                 For devices without this parameter you use the same value as tXSR
  '                 For some DDR-SDRAM data sheets, this parameter is known as tXSNR
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080038"
  Data_SetDWord "00000008"
End If

'Initialize Dynamic Memory Write Recovery Time Register (MPMCDynamictWR - 0x3108 0044)
'Bit 3:0 = 2_0001 ; Write recovery time(tWR) -> 2 clock cycles
'                 This value is normally found in SDRAM data sheets as tWR, tDPL, tRWL, or tRDL
Data_DestSpace "CODE & DATA"
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 Data_DestAddr "31080044"
 Data_SetDWord "00000001"

 If ( hclk <= 13) Then
  'Initialize Dynamic Memory Active To Active Command Period Register (MPMCDynamictRC - 0x3108
0048)
  'Bit 4:0 = 2_00001 ; Active to active Command period(tRC) -> 2 clock cycles
  '               This value is normally found in SDRAM data sheets as tRC
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080048"
  Data_SetDWord "00000001"
 ElseIf ( hclk > 13) And ( hclk <= 26) Then
  'Initialize Dynamic Memory Active To Active Command Period Register (MPMCDynamictRC - 0x3108
0048)
  'Bit 4:0 = 2_00010 ; Active to active Command period(tRC) -> 3 clock cycles
  '               This value is normally found in SDRAM data sheets as tRC
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080048"
  Data_SetDWord "00000002"
 ElseIf ( hclk > 26) And ( hclk <= 39) Then
  'Initialize Dynamic Memory Active To Active Command Period Register (MPMCDynamictRC - 0x3108
0048)
  'Bit 4:0 = 2_00011 ; Active to active Command period(tRC) -> 4 clock cycles
  '               This value is normally found in SDRAM data sheets as tRC
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080048"
  Data_SetDWord "00000003"
 ElseIf ( hclk > 39) And ( hclk <= 52) Then
  'Initialize Dynamic Memory Active To Active Command Period Register (MPMCDynamictRC - 0x3108
0048)
  'Bit 4:0 = 2_00100 ; Active to active Command period(tRC) -> 5 clock cycles
  '               This value is normally found in SDRAM data sheets as tRC
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080048"
  Data_SetDWord "00000004"
 ElseIf ( hclk > 52) And ( hclk <= 65) Then
  'Initialize Dynamic Memory Active To Active Command Period Register (MPMCDynamictRC - 0x3108
0048)
  'Bit 4:0 = 2_00101 ; Active to active Command period(tRC) -> 6 clock cycles
  '               This value is normally found in SDRAM data sheets as tRC
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080048"
  Data_SetDWord "00000005"
 ElseIf ( hclk > 65) And ( hclk <= 78) Then
  'Initialize Dynamic Memory Active To Active Command Period Register (MPMCDynamictRC - 0x3108
0048)
  'Bit 4:0 = 2_00110 ; Active to active Command period(tRC) -> 7 clock cycles
  '               This value is normally found in SDRAM data sheets as tRC
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080048"
  Data_SetDWord "00000006"
 ElseIf ( hclk > 78) And ( hclk <= 91) Then
  'Initialize Dynamic Memory Active To Active Command Period Register (MPMCDynamictRC - 0x3108
0048)
  'Bit 4:0 = 2_00111 ; Active to active Command period(tRC) -> 8 clock cycles
  '               This value is normally found in SDRAM data sheets as tRC
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   Data_DestSpace "CODE & DATA"
   Data_DestAddr "31080048"
   Data_SetDWord "00000007"
  Else
   'Initialize Dynamic Memory Active To Active Command Period Register (MPMCDynamictRC - 0x3108
0048)
   'Bit 4:0 = 2_01000 ; Active to active Command period(tRC) -> 9 clock cycles
   '               This value is normally found in SDRAM data sheets as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "31080048"
   Data_SetDWord "00000008"
  End If

  If ( hclk <= 13) Then
   'Initialize Dynamic Memory Auto-refresh Period Register (MPMCDynamictRFC - 0x3108 004C)
   'Bit 4:0 = 2_00001 ; Auto-refresh period and auto-refresh To active Command period(tRFC) -> 2 clock
cycles
   '               This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "3108004C"
   Data_SetDWord "00000001"
  ElseIf ( hclk > 13) And ( hclk <= 26) Then
   'Initialize Dynamic Memory Auto-refresh Period Register (MPMCDynamictRFC - 0x3108 004C)
   'Bit 4:0 = 2_00010 ; Auto-refresh period and auto-refresh To active Command period(tRFC) -> 3 clock
cycles
   '               This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "3108004C"
   Data_SetDWord "00000002"
  ElseIf ( hclk > 26) And ( hclk <= 39) Then
   'Initialize Dynamic Memory Auto-refresh Period Register (MPMCDynamictRFC - 0x3108 004C)
   'Bit 4:0 = 2_00011 ; Auto-refresh period and auto-refresh To active Command period(tRFC) -> 4 clock
cycles
   '               This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "3108004C"
   Data_SetDWord "00000003"
  ElseIf ( hclk > 39) And ( hclk <= 52) Then
   'Initialize Dynamic Memory Auto-refresh Period Register (MPMCDynamictRFC - 0x3108 004C)
   'Bit 4:0 = 2_00100 ; Auto-refresh period and auto-refresh To active Command period(tRFC) -> 5 clock
cycles
   '               This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "3108004C"
   Data_SetDWord "00000004"
  ElseIf ( hclk > 52) And ( hclk <= 65) Then
   'Initialize Dynamic Memory Auto-refresh Period Register (MPMCDynamictRFC - 0x3108 004C)
   'Bit 4:0 = 2_00101 ; Auto-refresh period and auto-refresh To active Command period(tRFC) -> 6 clock
cycles
   '               This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "3108004C"
   Data_SetDWord "00000005"
  ElseIf ( hclk > 65) And ( hclk <= 78) Then
   'Initialize Dynamic Memory Auto-refresh Period Register (MPMCDynamictRFC - 0x3108 004C)
```

```
   'Bit 4:0 = 2_00110 ; Auto-refresh period and auto-refresh To active Command period(tRFC) -> 7 clock
cycles
   '                This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "3108004C"
   Data_SetDWord "00000006"
  ElseIf ( hclk > 78) And ( hclk <= 91) Then
   'Initialize Dynamic Memory Auto-refresh Period Register (MPMCDynamictRFC - 0x3108 004C)
   'Bit 4:0 = 2_00111 ; Auto-refresh period and auto-refresh To active Command period(tRFC) -> 8 clock
cycles
   '                This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "3108004C"
   Data_SetDWord "00000007"
  Else
   'Initialize Dynamic Memory Auto-refresh Period Register (MPMCDynamictRFC - 0x3108 004C)
   'Bit 4:0 = 2_01000 ; Auto-refresh period and auto-refresh To active Command period(tRFC) -> 9 clock
cycles
   '                This value is normally found in SDRAM data sheets as tRFC, or sometimes as tRC
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "3108004C"
   Data_SetDWord "00000008"
  End If

  If ( hclk <= 13) Then
   'Initialize Dynamic Memory Exit Self-refresh Register (MPMCDynamictXSR - 0x3108 0050)
   'Bit 7:0 = 2_00000001 ; Exit self-refresh to active Command Time(tXSR) -> 2 clock cycles
   '                  This value is normally found in SDRAM data sheets as tXSR
   '                  But it is sometimes called tXSNR in some DDR SDRAM data sheets.
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "31080050"
   Data_SetDWord "00000001"
  ElseIf ( hclk > 13) And ( hclk <= 26) Then
   'Initialize Dynamic Memory Exit Self-refresh Register (MPMCDynamictXSR - 0x3108 0050)
   'Bit 7:0 = 2_00000010 ; Exit self-refresh to active Command Time(tXSR) -> 3 clock cycles
   '                  This value is normally found in SDRAM data sheets as tXSR
   '                  But it is sometimes called tXSNR in some DDR SDRAM data sheets.
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "31080050"
   Data_SetDWord "00000002"
  ElseIf ( hclk > 26) And ( hclk <= 39) Then
   'Initialize Dynamic Memory Exit Self-refresh Register (MPMCDynamictXSR - 0x3108 0050)
   'Bit 7:0 = 2_00000011 ; Exit self-refresh to active Command Time(tXSR) -> 4 clock cycles
   '                  This value is normally found in SDRAM data sheets as tXSR
   '                  But it is sometimes called tXSNR in some DDR SDRAM data sheets.
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "31080050"
   Data_SetDWord "00000003"
  ElseIf ( hclk > 39) And ( hclk <= 52) Then
   'Initialize Dynamic Memory Exit Self-refresh Register (MPMCDynamictXSR - 0x3108 0050)
   'Bit 7:0 = 2_00000100 ; Exit self-refresh to active Command Time(tXSR) -> 5 clock cycles
   '                  This value is normally found in SDRAM data sheets as tXSR
   '                  But it is sometimes called tXSNR in some DDR SDRAM data sheets.
   Data_DestSpace "CODE & DATA"
   Data_DestAddr "31080050"
   Data_SetDWord "00000004"
```

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  ElseIf ( hclk > 52) And ( hclk <= 65) Then
    'Initialize Dynamic Memory Exit Self-refresh Register (MPMCDynamictXSR - 0x3108 0050)
    'Bit 7:0 = 2_00000101 ; Exit self-refresh to active Command Time(tXSR) -> 6 clock cycles
    '                  This value is normally found in SDRAM data sheets as tXSR
    '                  But it is sometimes called tXSNR in some DDR SDRAM data sheets.
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080050"
    Data_SetDWord "00000005"
  ElseIf ( hclk > 65) And ( hclk <= 78) Then
    'Initialize Dynamic Memory Exit Self-refresh Register (MPMCDynamictXSR - 0x3108 0050)
    'Bit 7:0 = 2_00000110 ; Exit self-refresh to active Command Time(tXSR) -> 7 clock cycles
    '                  This value is normally found in SDRAM data sheets as tXSR
    '                  But it is sometimes called tXSNR in some DDR SDRAM data sheets.
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080050"
    Data_SetDWord "00000006"
  ElseIf ( hclk > 78) And ( hclk <= 91) Then
    'Initialize Dynamic Memory Exit Self-refresh Register (MPMCDynamictXSR - 0x3108 0050)
    'Bit 7:0 = 2_00000111 ; Exit self-refresh to active Command Time(tXSR) -> 8 clock cycles
    '                  This value is normally found in SDRAM data sheets as tXSR
    '                  But it is sometimes called tXSNR in some DDR SDRAM data sheets.
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080050"
    Data_SetDWord "00000007"
  Else
    'Initialize Dynamic Memory Exit Self-refresh Register (MPMCDynamictXSR - 0x3108 0050)
    'Bit 7:0 = 2_00001000 ; Exit self-refresh to active Command Time(tXSR) -> 9 clock cycles
    '                  This value is normally found in SDRAM data sheets as tXSR
    '                  But it is sometimes called tXSNR in some DDR SDRAM data sheets.
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080050"
    Data_SetDWord "00000008"
  End If

  If ( hclk <= 13) Then
    'Initialize Dynamic Memory Active Bank A to Active Bank B Time Register (MPMCDynamictRRD -
0x3108 0054)
    'Bit 3:0 = 2_0000 ; Active bank A to active bank B latency(tRRD) -> 1 clock cycles
    '                This value is normally found in SDRAM data sheets as tRRD
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080054"
    Data_SetDWord "00000000"
  ElseIf ( hclk > 13) And ( hclk <= 26) Then
    'Initialize Dynamic Memory Active Bank A to Active Bank B Time Register (MPMCDynamictRRD -
0x3108 0054)
    'Bit 3:0 = 2_0000 ; Active bank A to active bank B latency(tRRD) -> 1 clock cycles
    '                This value is normally found in SDRAM data sheets as tRRD
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080054"
    Data_SetDWord "00000000"
  ElseIf ( hclk > 26) And ( hclk <= 39) Then
    'Initialize Dynamic Memory Active Bank A to Active Bank B Time Register (MPMCDynamictRRD -
0x3108 0054)
    'Bit 3:0 = 2_0000 ; Active bank A to active bank B latency(tRRD) -> 1 clock cycles
    '                This value is normally found in SDRAM data sheets as tRRD
    Data_DestSpace "CODE & DATA"
```

```
    Data_DestAddr "31080054"
    Data_SetDWord "00000000"
  ElseIf ( hclk > 39) And ( hclk <= 52) Then
    'Initialize Dynamic Memory Active Bank A to Active Bank B Time Register (MPMCDynamictRRD -
0x3108 0054)
    'Bit 3:0 = 2_0000 ; Active bank A to active bank B latency(tRRD) -> 1 clock cycles
    '               This value is normally found in SDRAM data sheets as tRRD
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080054"
    Data_SetDWord "00000000"
  ElseIf ( hclk > 52) And ( hclk <= 65) Then
    'Initialize Dynamic Memory Active Bank A to Active Bank B Time Register (MPMCDynamictRRD -
0x3108 0054)
    'Bit 3:0 = 2_0001 ; Active bank A to active bank B latency(tRRD) -> 2 clock cycles
    '               This value is normally found in SDRAM data sheets as tRRD
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080054"
    Data_SetDWord "00000001"
  ElseIf ( hclk > 65) And ( hclk <= 78) Then
    'Initialize Dynamic Memory Active Bank A to Active Bank B Time Register (MPMCDynamictRRD -
0x3108 0054)
    'Bit 3:0 = 2_0001 ; Active bank A to active bank B latency(tRRD) -> 2 clock cycles
    '               This value is normally found in SDRAM data sheets as tRRD
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080054"
    Data_SetDWord "00000001"
  ElseIf ( hclk > 78) And ( hclk <= 91) Then
    'Initialize Dynamic Memory Active Bank A to Active Bank B Time Register (MPMCDynamictRRD -
0x3108 0054)
    'Bit 3:0 = 2_0001 ; Active bank A to active bank B latency(tRRD) -> 2 clock cycles
    '               This value is normally found in SDRAM data sheets as tRRD
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080054"
    Data_SetDWord "00000001"
  Else
    'Initialize Dynamic Memory Active Bank A to Active Bank B Time Register (MPMCDynamictRRD -
0x3108 0054)
    'Bit 3:0 = 2_0001 ; Active bank A to active bank B latency(tRRD) -> 2 clock cycles
    '               This value is normally found in SDRAM data sheets as tRRD
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080054"
    Data_SetDWord "00000001"
  End If

  'Initialize Dynamic Memory Load Mode Register To Active Command Time (MPMCDynamictMRD -
0x3108 0058)
  'Bit 3:0 = 2_0001 ; Load mode register to active Command Time(tMRD) -> 2 clock cycles
  '               This value is normally found in SDRAM data sheets as tMRD, or tRSA
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080058"
  Data_SetDWord "00000001"

  'Initialize Dynamic Memory Last Data In to Read Command Time (MPMCDynamicCDLR - 0x3108
005C)
  'Bit 3:0 = 2_0000 ; Last data in to read command time (tCDLR) -> 1 clock cycles
  '               This value is normally found in SDRAM data sheets as tCDLR
```

```
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "3108005C"
  Data_SetDWord "00000000"

  'Initialize Dynamic Memory Control Register (MPMCDynamicControl - 0x3108 0020)
  'Bit 0 = 2_1 ; Dynamic memory clock enable(CE) -> All clock enables are driven HIGH continuously
  'Bit 1 = 2_1 ; Dynamic memory clock control(CS) -> RAM_CLK runs continuously
  'Bit 2 = 2_0 ; Self-refresh request, MPMCSREFREQ(SR) -> Normal mode
  'Bit 3 = 2_0 ; Self-Refresh Clock Control(SRMCC) -> RAM_CLK and DDR_nCLK run continuously
during self-refresh mode
  'Bit 4 = 2_1 ; Inverted Memory Clock Control(IMCC) -> DDR_nCLK disabled
  'Bit 5 = 2_0 ; Memory clock control(MMC) -> RAM_CLK enabled (POR reset value)
  'Bit 8:7 = 2_11 ; SDRAM initialization(I) -> Issue SDRAM NOP (no operation) command
  'Bit 13 = 2_0 ; Low-power SDRAM deep-sleep mode(DP) -> Normal operation
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080020"
  Data_SetDWord "00000193"

  'Wait for 1 second
  Wait 1

  'Initialize Dynamic Memory Control Register (MPMCDynamicControl - 0x3108 0020)
  'Bit 0 = 2_1 ; Dynamic memory clock enable(CE) -> All clock enables are driven HIGH continuously
  'Bit 1 = 2_1 ; Dynamic memory clock control(CS) -> RAM_CLK runs continuously
  'Bit 2 = 2_0 ; Self-refresh request, MPMCSREFREQ(SR) -> Normal mode
  'Bit 3 = 2_0 ; Self-Refresh Clock Control(SRMCC) -> RAM_CLK and DDR_nCLK run continuously
during self-refresh mode
  'Bit 4 = 2_1 ; Inverted Memory Clock Control(IMCC) -> DDR_nCLK disabled
  'Bit 5 = 2_0 ; Memory clock control(MMC) -> RAM_CLK enabled (POR reset value)
  'Bit 8:7 = 2_10 ; SDRAM initialization(I) -> Issue SDRAM PALL (precharge all) command
  'Bit 13 = 2_0 ; Low-power SDRAM deep-sleep mode(DP) -> Normal operation
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080020"
  Data_SetDWord "00000113"

  'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
  'Bit 10:0 = 2_00000000010 ; Refresh timer (REFRESH) -> 2 x 16 clocks between SDRAM refresh cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080024"
  Data_SetDWord "00000002"

  'Wait for 1 second
  Wait 1

  If ( hclk <= 13) Then
    'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
    'Bit 10:0 = 2_00000001100 ; Refresh timer (REFRESH) -> 12 x 16 clocks between SDRAM refresh
cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080024"
    Data_SetDWord "0000000C"
  ElseIf ( hclk > 13) And ( hclk <= 26) Then
    'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
    'Bit 10:0 = 2_00000011001 ; Refresh timer (REFRESH) -> 25 x 16 clocks between SDRAM refresh
cycles
    Data_DestSpace "CODE & DATA"
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    Data_DestAddr "31080024"
    Data_SetDWord "00000019"
  ElseIf ( hclk > 26) And ( hclk <= 39) Then
    'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
    'Bit 10:0 = 2_00000100011 ; Refresh timer (REFRESH) -> 35 x 16 clocks between SDRAM refresh
cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080024"
    Data_SetDWord "00000023"
  ElseIf ( hclk > 39) And ( hclk <= 52) Then
    'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
    'Bit 10:0 = 2_00000110011 ; Refresh timer (REFRESH) -> 51 x 16 clocks between SDRAM refresh
cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080024"
    Data_SetDWord "00000033"
  ElseIf ( hclk > 52) And ( hclk <= 65) Then
    'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
    'Bit 10:0 = 2_00001000000 ; Refresh timer (REFRESH) -> 64 x 16 clocks between SDRAM refresh
cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080024"
    Data_SetDWord "00000040"
  ElseIf ( hclk > 65) And ( hclk <= 78) Then
    'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
    'Bit 10:0 = 2_00001001101 ; Refresh timer (REFRESH) -> 77 x 16 clocks between SDRAM refresh
cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080024"
    Data_SetDWord "0000004D"
  ElseIf ( hclk > 78) And ( hclk <= 91) Then
    'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
    'Bit 10:0 = 2_00001011001 ; Refresh timer (REFRESH) -> 89 x 16 clocks between SDRAM refresh
cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080024"
    Data_SetDWord "00000059"
  Else
    'Initialize Dynamic Memory Refresh Timer Register (MPMCDynamicRefresh - 0x3108 0024)
    'Bit 10:0 = 2_00001100101 ; Refresh timer (REFRESH) -> 101 x 16 clocks between SDRAM refresh
cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080024"
    Data_SetDWord "00000065"
  End If

  If ( hclk <= 13) Then
    'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
    'Bit 3:0 = 2_0001 ; RAS latency(Active to Read/Write delay)(RAS) -> 1 clock cycles
    '               This value is normally found in SDRAM data sheets as tRCD
    'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
    Data_DestSpace "CODE & DATA"
    Data_DestAddr "31080104"
    Data_SetDWord "00000301"
  ElseIf ( hclk > 13) And ( hclk <= 26) Then
    'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
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  'Bit 3:0 = 2_0001 ; RAS latency(Active to Read/Write delay)(RAS) -> 1 clock cycles
  '                   This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000301"
ElseIf ( hclk > 26) And ( hclk <= 39) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0001 ; RAS latency(Active to Read/Write delay)(RAS) -> 1 clock cycles
  '                   This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000301"
ElseIf ( hclk > 39) And ( hclk <= 52) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0010 ; RAS latency(Active to Read/Write delay)(RAS) -> 2 clock cycles
  '                   This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000302"
ElseIf ( hclk > 52) And ( hclk <= 65) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0010 ; RAS latency(Active to Read/Write delay)(RAS) -> 2 clock cycles
  '                   This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000302"
ElseIf ( hclk > 65) And ( hclk <= 78) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0010 ; RAS latency(Active to Read/Write delay)(RAS) -> 2 clock cycles
  '                   This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000302"
ElseIf ( hclk > 78) And ( hclk <= 91) Then
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0010 ; RAS latency(Active to Read/Write delay)(RAS) -> 2 clock cycles
  '                   This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000302"
Else
  'Initialize Dynamic Memory RAS & CAS Delay Reg (MPMCDynamicRasCas0 - 0x3108 0104)
  'Bit 3:0 = 2_0011 ; RAS latency(Active to Read/Write delay)(RAS) -> 3 clock cycles
  '                   This value is normally found in SDRAM data sheets as tRCD
  'Bit 10:7 = 2_0110 ; CAS latency(CAS) -> Three clock cycles
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080104"
  Data_SetDWord "00000303"
End If
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  'Initialize Dynamic Memory Configuration Register (MPMCDynamicConfig0 - 0x3108 0100)
  'Bit 2:0 = 2_010 ; Memory device(MD) -> Low power SDR SDRAM
  'Bit 14:7 = 2_ 10101001 ; Address mapping(AM) -> 32-bit external bus low-power SDRAM address
mapping :
  '                                    128Mb (8Mx16), 4 banks, row length = 12, column length = 9
  'Bit 20 = 2_0 ; Write protect(P) -> Writes not protected
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080100"
  Data_SetDWord "00005482"

  'Initialize Dynamic Memory Control Register (MPMCDynamicControl - 0x3108 0020)
  'Bit 0 = 2_ 1 ; Dynamic memory clock enable(CE) -> All clock enables are driven HIGH continuously
  'Bit 1 = 2_ 1 ; Dynamic memory clock control(CS) -> RAM_CLK runs continuously
  'Bit 2 = 2_ 0 ; Self-refresh request, MPMCSREFREQ(SR) -> Normal mode
  'Bit 3 = 2_ 0 ; Self-Refresh Clock Control(SRMCC) -> RAM_CLK and DDR_nCLK run continuously
during self-refresh mode
  'Bit 4 = 2_ 1 ; Inverted Memory Clock Control(IMCC) -> DDR_nCLK disabled
  'Bit 5 = 2_ 0 ; Memory clock control(MMC) -> RAM_CLK enabled (POR reset value)
  'Bit 8:7 = 2_10 ; SDRAM initialization(I) -> Issue SDRAM MODE command
  'Bit 13 = 2_0 ; Low-power SDRAM deep-sleep mode(DP) -> Normal operation
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080020"
  Data_SetDWord "00000093"

  'Load Mode Register by reading the address location 0x8001 8000
  'Refer to Application Note for detail
  Data_SourceSpace "CODE & DATA"
  Data_SourceAddr "80018000"
  rslt = Data_GetDWord

  'Initialize Dynamic Memory Control Register (MPMCDynamicControl - 0x3108 0020)
  'Bit 0 = 2_ 1 ; Dynamic memory clock enable(CE) -> All clock enables are driven HIGH continuously
  'Bit 1 = 2_ 1 ; Dynamic memory clock control(CS) -> RAM_CLK runs continuously
  'Bit 2 = 2_ 0 ; Self-refresh request, MPMCSREFREQ(SR) -> Normal mode
  'Bit 3 = 2_ 0 ; Self-Refresh Clock Control(SRMCC) -> RAM_CLK and DDR_nCLK run continuously
during self-refresh mode
  'Bit 4 = 2_ 1 ; Inverted Memory Clock Control(IMCC) -> DDR_nCLK disabled
  'Bit 5 = 2_ 0 ; Memory clock control(MMC) -> RAM_CLK enabled (POR reset value)
  'Bit 8:7 = 2_10 ; SDRAM initialization(I) -> Issue SDRAM MODE command
  'Bit 13 = 2_0 ; Low-power SDRAM deep-sleep mode(DP) -> Normal operation
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080020"
  Data_SetDWord "00000093"

  'Load Extended Mode Register by reading the address location 0x8102 C000
  'Refer to Application Note for detail
  Data_SourceSpace "CODE & DATA"
  Data_SourceAddr "8102C000"
  rslt = Data_GetDWord

  'Initialize Dynamic Memory Control Register (MPMCDynamicControl - 0x3108 0020)
  'Bit 0 = 2_ 0 ; Dynamic memory clock enable(CE) -> clock enable of idle devices are deasserted to save
power
  'Bit 1 = 2_ 0 ; Dynamic memory clock control(CS) -> RAM_CLK stops when all SDRAMs are idle and
during self-refresh mode
  'Bit 2 = 2_ 0 ; Self-refresh request, MPMCSREFREQ(SR) -> Normal mode
```

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  'Bit 3 = 2_ 0 ; Self-Refresh Clock Control(SRMCC) -> RAM_CLK and DDR_nCLK run continuously
during self-refresh mode
  'Bit 4 = 2_ 1 ; Inverted Memory Clock Control(IMCC) -> DDR_nCLK disabled
  'Bit 5 = 2_ 0 ; Memory clock control(MMC) -> RAM_CLK enabled (POR reset value)
  'Bit 8:7 = 2_00 ; SDRAM initialization(I) -> Issue SDRAM NORMAL operation command
  'Bit 13 = 2_0 ; Low-power SDRAM deep-sleep mode(DP) -> Normal operation
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080020"
  Data_SetDWord "00000010"

  'Initialize SDRAM Controller AHB Timeout Registers (MPMCAHBTime0 - 0x3108 0408)
  'Bit 9:0 = 2_0001100100 ; AHB Timeout (AHBTIMEOUT) -> Number of AHB cycles before timeout is
reached = 100
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080408"
  Data_SetDWord "00000064"

  'Initialize SDRAM Controller AHB Timeout Registers (MPMCAHBTime2 - 0x3108 0448)
  'Bit 9:0 = 2_0110010000 ; AHB Timeout (AHBTIMEOUT) -> Number of AHB cycles before timeout is
reached = 400
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080448"
  Data_SetDWord "00000190"

  'Initialize SDRAM Controller AHB Timeout Registers (MPMCAHBTime3 - 0x3108 0468)
  'Bit 9:0 = 2_0110010000 ; AHB Timeout (AHBTIMEOUT) -> Number of AHB cycles before timeout is
reached = 400
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080468"
  Data_SetDWord "00000190"

  'Initialize SDRAM Controller AHB Timeout Registers (MPMCAHBTime4 - 0x3108 0488)
  'Bit 9:0 = 2_0110010000 ; AHB Timeout (AHBTIMEOUT) -> Number of AHB cycles before timeout is
reached = 400
  Data_DestSpace "CODE & DATA"
  Data_DestAddr "31080488"
  Data_SetDWord "00000190"

  File_Refresh
End Sub
```