MC9S12T64 CPU Module Jumpers

Version 2.2
March 26, 2003

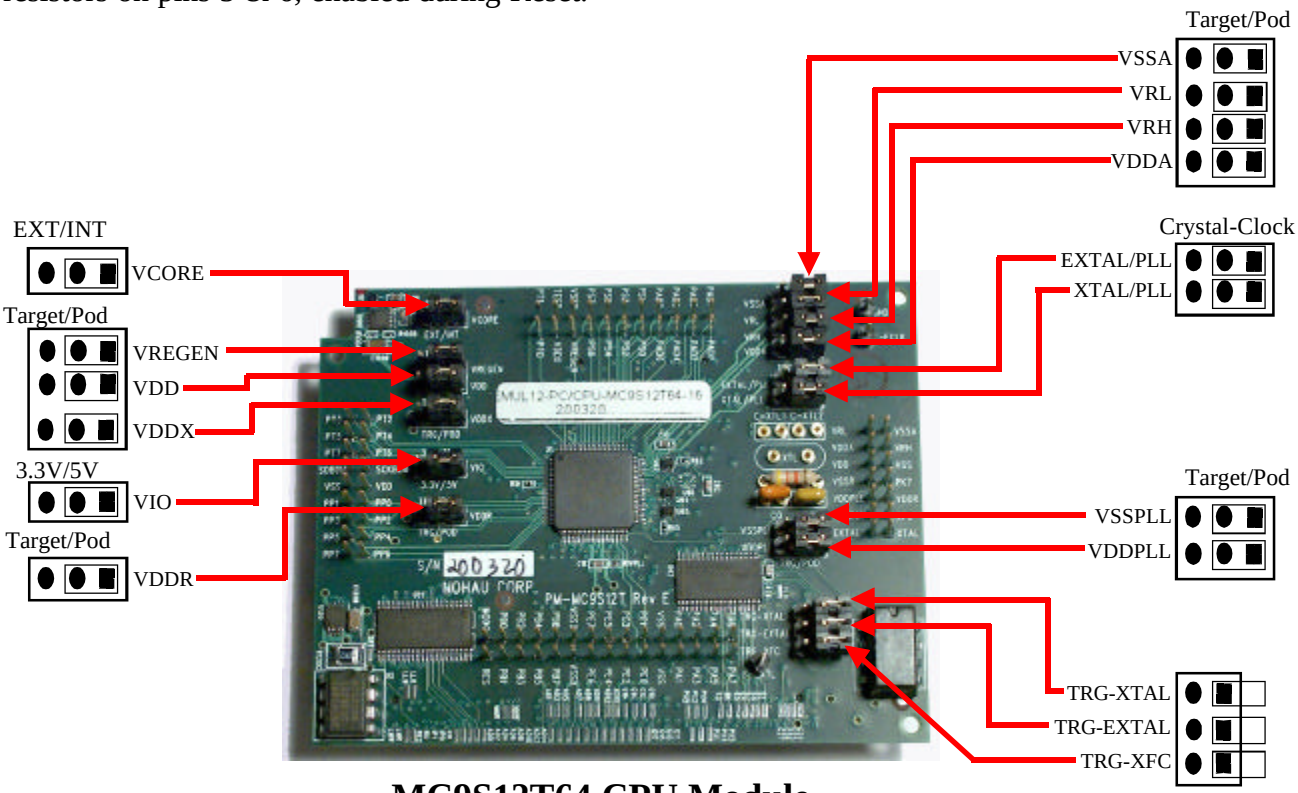
The following is a photo of the MC9S12T64 CPU module which depicts the jumper configurations. The default setting is for all the voltages, chip power supplies and ground being connected to the pod which is position 1 and 2 on the jumpers. To have these voltages or grounds connected to the target, switch the appropriate jumpers to pins 2 and 3.

Note 1: To set the VIO jumper to 3.3 volts, 2.5 volts should be supplied to VDD and VDDPLL from an external supply. This can be achieved by also setting the VCORE jumper to the External position.

Note 2: The default setting of the I/O voltage is 5 volts.

Note 3: On the T64 MCU the PPAGE register value cannot be changed on Normal and Emulation operating modes. This T64 limitation applies to both PPAGE writes as well as CALL and RTC instruction execution. As a result, the T64 emulator behaves similarly, and ignores writes to PPAGE to maintain its value 3CH always.

Note 4: The emulator PORT E pins 0 and 1, always have pull-up resistors enabled (approximately 30Kohm), regardless of the state of the PUPE bit in the PUCR register. The behavior of all other PORT E pins is as expected: Pull ups on pins 2,3,4 & 7 controlled by the PUPE bit, and pull-down resistors on pins 5 & 6, enabled during Reset.



MC9S12T64 CPU Module

* Please note that page six of this document is a schematic representation of the jumpers on the module.

Descriptions for the Jumpers, Pin Sockets and Test Points

Jumpers

VCORE-EXT/INT: selects if 2.5V for the CPU VDD and VDDPLL should be generated by the internal CPU voltage regulator or an external 2.5V regulator. This jumper has meaning only when the VREGEN jumper is in the POD position. The default position is INT.

VREGEN-Target/Pod: selects if the CPU VREGEN pin should be driven by the target VREGEN pin, or by the POD VCORE jumper. The default position is POD. When VREGEN is driven low, the internal CPU 2.5V regulator is turned off and an external 2.5V supply should be used to power the VDD and VDDPLL. In this case of VREGEN low, when the VDD and the VDDPLL jumpers are in the POD position, a 2.5V regulator on the POD will be turned on and will supply the needed power to the VDD and VDDPLL. If the VDD and VDDPLL jumpers are in the Target position and VREGEN is low, the target will need to supply 2.5V to VDD and VDDPLL. The default condition is VREGEN is driven high by the VCORE jumper, and the internal CPU 2.5V regulator is on.

VIO-3.3V/5V: selects if the 5 volts or 3.3 volts should be applied to VDDX, VDDR, VDDA and VRH. This jumper sets VDDX, VDDR, VDDA and VRH voltages only when the appropriate VDDX, VDDR, VDDA and VRH jumpers are in the POD position. Please note that in the case of the T64, if 3.3V is selected, the internal CPU 2.5V regulator should be turned off and an external 2.5V supply should be used to power VDD and VDDPLL. The default position of this jumper is 5V.

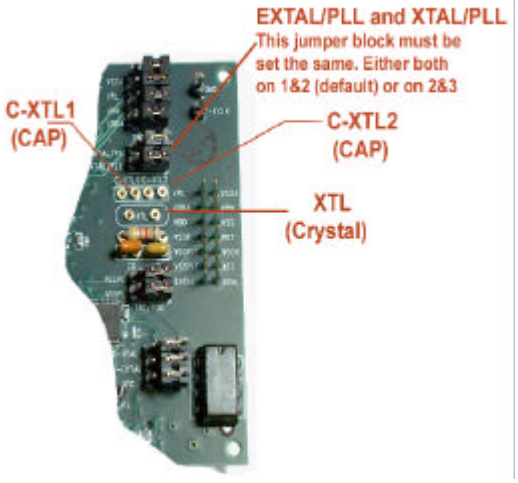
VDDX, VDDR-Target/Pod: selects if VDDX and VDDR should be powered by the POD as selected by the VIO jumper, or by the target power. The default position is POD. Please note that VDDX is also used to power the port replacement unit (PRU) which regenerates ports A, B, E and K and therefor consumes higher current then normal- if powered by the target requires slightly increased current.

VDDA, VRH-Target/Pod: select if VDDA and VRH are powered by the POD as selected by the VIO jumper or by the target power. The default position is POD.

VDD, VDDPLL-Target/Pod: VDD and VDDPLL are generated by default by the internal CPU 2.5V regulator. In this default case, these jumpers select if the POD capacitors or the target capacitors will be connected to these CPU pins. In case the internal CPU 2.5V is disabled, these jumpers select if VDD and VDDPLL are powered by the POD generated 2.5V or by the target generated 2.5V. The default position is POD.

VSSA, VRL, VSSPLL-Target/Pod: selects if VSSA, VRL and VSSPLL should be connected to the POD ground or should be connected to the target to allow applying different voltages to each of these CPU pins. The default position is POD.

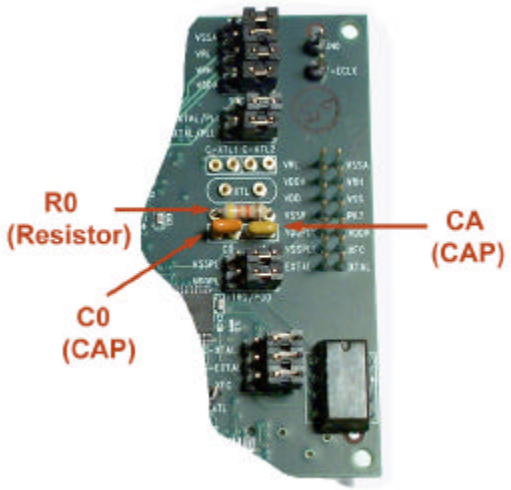
Jumpers (continued)



EXTAL/PLL, XTAL/PLL: these two jumpers should both be set to the same position. When both are set to the PLL position, the POD PLL will be used to drive a 2.5V square wave clock frequency to the EXTAL pin of the CPU. The POD PLL is automatically configured by Seehau for the value entered in the clock field of the emulator configuration window to generate any desired frequency (worst case accuracy of less then 1%). When the jumpers are set to the EXTAL and XTAL positions, a Colpitts crystal and capacitors are mounted in XTL, C-XTL1 and C-XTL2 as shown in the photo to the right. In this EXTAL and XTAL position, feeding the operating frequency from the target is also possible by installing the jumpers on the TRG-EXTAL and TRG-XTAL and making sure that the XTL, C-XTL1 and C-XTL2 pin sockets are un-populated. The default position for both of these jumpers is PLL. It is not recommended to drive the analog EXTAL and XTAL signals from the target as they will be susceptible to noise due to the long distance.

TRG-EXTAL, TRG-XTAL: these two-pin jumpers have meaning only when the EXTAL/PLL and XTAL/PLL jumpers are in the EXTAL and XTAL positions. When the TRG-EXTAL and TRG-XTAL jumpers are installed, a target crystal or clock generator can be used to drive the CPU EXTAL and XTAL pins. When these jumpers are on, no components should be installed on the XTL, C-XTL1 and C-XTL2 pin sockets on the CPU module. The default position of these jumpers is jumper off. It is not recommended to drive the analog EXTAL and XTAL signals from the target as they will be susceptible to noise due to the long distance.

TRG-XFC: when installed, this two-pin jumper allows the target PLL filter circuit to connect to the XFC pin of the CPU. When this jumper in on, no components should be installed on the R0, C0 and CA pin sockets on the CPU module. When this jumper is off, the R0, C0 and CA pin sockets can be populated with components to form the PLL filter to connect to the CPU XFC pin (these pin sockets are populated with components by default). The default position of the TRG-XFC jumper is jumper off.



Jumpers on the Emulator Motherboard

ECLK jumper on the emulator motherboard- PE4/FAST-ECLK: this jumper selects between driving the target PE4 pin by the port replacement unit PE4 signal, or by a fast ECLK signal which can be used to optimize the target bus timing for expanded mode applications by 2.5nSEC. For single-chip mode applications the PE4 position should be used and for expanded-mode applications the FAST-ECLK position is recommended. The default position is PE4.

EPC jumper on the emulator motherboard: this jumper should be on when using the EPC parallel port or the USB communication interfaces to the PC.

Pin Sockets

R0, C0 and CA pin sockets on the CPU module: these pin sockets are used to install the R0, C0 and CA components of the PLL loop filter that connect to the CPU XFC pin. The PLL loop filter is required in order to allow the use of the internal CPU PLL. Since XFC is an analog signal which is susceptible to noise, it is recommended to install the PLL loop filter components on these pin sockets close to the CPU XFC pin. When components are installed in these pin sockets the TRG-XFC jumper must be off. These pin sockets are installed with default components that we have found to perform well for a wide range of PLL frequencies. These default components are:

R0=43K
C0=1nF
CA=100pF

Connecting PLL loop filter components on the target to the XFC pin of the CPU on the CPU module is not recommended. However, if desired it can be implemented by taking off the installed components on the R0, C0 and CA pin sockets on the CPU module and installing the TRG-XFC jumper in the on position.

XTL, C-XTL1 and C-XTL2 pin sockets on the CPU module: these pin sockets can be used to install user specified Colpitts configuration crystal components close to the CPU to be connected to the CPU EXTAL and XTAL pins. When such components are installed the EXTAL/PLL and XTAL/PLL jumpers should be in the EXTAL and XTAL position and the TRG-EXTAL and TRG-XTAL jumpers should be off. Since EXTAL and XTAL are analog signals with reduced voltage swing in the case of Colpitts crystal configuration and are susceptible to noise, it is recommend to install the Colpitts crystal components on these pin sockets close to the CPU EXTAL and XTAL pins.

Test Points

GND-ground test points: can be used to connect ground to external measuring devices such as scope, logic analyzer, etc.

F-ECLK: this test point can be used to measure a buffered ECLK signal. It can be used to measure the bus speed and has a voltage swing of 0 - 3.3V.

F-EXTL: this test point can be used to measure the POD PLL generated frequency. This signal is also used to drive the CPU clock in the default jumpers setup. The frequency on the test point is required to be equal (with low allowed deviation) to the actual frequency driven to the CPU EXTAL pin.

GND-TP on the emulator motherboard: additional ground test point. Can be used to connect ground to external measuring devices such as scope, logic analyzer, etc..

VCC-TP on the emulator motherboard: can be used to measure 5V main supply of the emulator system.